Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method, ~~for~~

synchronising start of cell times in input/output ~~means~~ circuits with cell transmission periods in ~~at least one~~ a cross-connection ~~means for packet switching~~ circuit,

~~where~~ transferring cells ~~are transferred~~ between said input/output ~~means~~ circuits by said cross-connection ~~means~~ circuit in cell transfer periods,

~~where~~ changing configurations of said cross-connection ~~means are changed~~ circuit between cell transfer periods in cross-connection configuration periods,

~~where~~ sending cells from a sending input/output circuit of said input/output ~~means are sent~~ circuits at start of cell times, ~~and~~

~~where~~ receiving said sent cells ~~are received~~ in said cross-connection circuit~~means~~, ~~characterized by~~ wherein changing configurations includes oscillating said ~~configuration~~ configurations between a loopback configuration and a no-transmission configuration during a set up period,

~~whereby~~ transferring received cells ~~are transferred~~ back to said sending input/output ~~means~~ circuit in said loopback configuration and not transferring received cells ~~are not transferred~~ back to said sending input/output ~~means~~ circuit in said no-transmission configuration,

receiving back transferred cells in said sending input/output ~~means~~ circuit,

checking said received cells in said sending input/output ~~means~~ circuit for a transmission error,

shifting an offset of said start cell times in case a transmission error occurred,

until transferring back at least one cell is wholly carried out within a cell transfer period.

2. (Currently Amended) A method according to claim 1, ~~characterized by~~wherein the shifting includes shifting said offset of start of cell times in said sending input/output ~~means~~circuit, respectively, to align the time sent cells from said sending input/output ~~means~~ circuit are received in said cross-connection circuit~~means~~.

3. (Currently Amended) A method according to claim 1, ~~characterized by~~including controlling said start of cell times, said offset of start of cell times and said cross-connection configuration times by a central clock signal.

4. (Currently Amended) A method according to claim 1, ~~characterized by~~including calculating start of cell times based on a start of cell signal and said offset of said start of cell times, serialising said cells, and sending said serialised cells together with said start of cell signal at said start of cell times.

5. (Currently Amended) A method according to claim 1, ~~characterized by~~including receiving transferred back cells, de-serialising said cells and checking each cell for transmission errors.

6. (Currently Amended) A method according to claim 1, ~~characterized by~~including receiving transferred back cells, de-serialising said cells and evaluating a bit error indicator.

7. (Currently Amended) A method according to claim 3, ~~characterized by~~wherein the shifting includes shifting said offset of start of cell times using an offset counter and changing said offset counter by an amount of clock cycles of said central clock signal.

8. (Currently Amended) A method according to claim 1, ~~characterized by~~ wherein the shifting includes shifting said offset of said start of cell times to a maximum without

generating transmission errors, and shifting said offset of said start of cell times to a minimum without generating transmission errors.

9. (Currently Amended) A method according to claim 8, ~~characterized by~~ wherein the shifting includes setting said offset of said start of cell times in between said maximum and said minimum.

10. (Currently Amended) A packet switch comprising:

~~input/output means with~~ a plurality of port ~~controller~~ controllers each with a cell input port and a cell output port, and

cross-connection means ~~comprising~~ including cell input ports and cell output ports connected to said cell output ~~port~~ ports and cell input ~~port~~ ports of said port controllers, respectively,

~~characterized in that said~~ wherein a sending port controller of said port controllers comprises:

a start of cell signal generator for generating start of cell signals,

an offset controller for shifting a start of cell time based on said start of cell signal, and

an error detection means for detecting corrupt received cells, and

~~that~~ wherein said cross-connection means comprises:

a configuration controller for controlling an oscillation between a loopback configuration and a no-transmission configuration of said cross-connection means.

11. (Currently Amended) A packet switch according to claim 10, ~~characterized in that~~further comprising a central clock generator ~~is provided~~ for providing a central clock signal, ~~and that~~wherein said start of cell signal generator, said offset controller, and said configuration controller each comprise an input port for said central clock signal.

12. (Currently Amended) A packet switch according to claim 10, ~~characterized in that~~wherein said sending port controller comprises a serialiser and a de-serialiser for serialising cells to be sent and de-serialising received cells.

13. (Currently Amended) A packet switch according to claim 10, ~~characterized in that~~wherein said cross-connection means comprise a N × N crossbar matrix, selectively connecting N cell input ports with N cell output ports.

14. (Currently Amended) A packet switch according to claim 13, ~~characterized in that~~wherein said loopback configuration is realised by a unit matrix and a no-transmission configuration is realised by a null matrix.

15. (Currently Amended) A packet switch according to claim 10, ~~characterized in that~~wherein said error detection means is a bit error indicator.

16. (Currently Amended) ~~Use of a~~A method, comprising: ~~according to claim 1~~

synchronizing start of cell times, in a packet switched ~~network for synchronising start of cell times in various~~ network, for plural port controllers during a set up to allow configuration changes in a cross-connection ~~means~~ circuit without disturbing cell transfers;

transferring cells between said port controllers by said cross-connection circuit in cell transfer periods;

changing configurations of said cross-connection circuit between cell transfer periods in cross-connection configuration periods;

sending cells from a sending port controller of said port controllers at start of cell times;

receiving said sent cells in said cross-connection circuit, wherein changing configurations includes oscillating said configurations between a loopback configuration and a no-transmission configuration during a set up period;

transferring received cells back to said sending port controller in said loopback configuration and not transferring received cells back to said sending port controller in said no-transmission configuration;

receiving back transferred cells in said sending port controller;

checking said received cells in said sending port controller for a transmission error; and

shifting an offset of said start cell times in case a transmission error occurred, until transferring back at least one cell is wholly carried out within a cell transfer period.

17. (Canceled)

18. (New) A method according to claim 16, wherein the shifting includes shifting said offset of start of cell times in said sending port controller, respectively, to align the time sent cells from said sending input/output circuit are received in said cross-connection circuit.

19. (New) A method according to claim 16, including controlling said start of cell times, said offset of start of cell times and said cross-connection configuration times by a central clock signal.

20. (New) A method, comprising:

synchronising start of cell times in a plurality of port controllers during a set up to allow configuration changes in a cross-connection circuit without disturbing cell transfers, the port controllers each having a cell input port and a cell output port, and the cross-connection circuit including cell input ports and cell output ports connected to said cell output ports and cell input ports of said port controllers, respectively,

wherein a sending port controller of said port controllers performs:

generating start of cell signals using a start of cell signal generator,

shifting a start of cell time based on said start of cell signal using an offset controller, and

detecting corrupt received cells using an error detector, and

wherein said cross-connection controls an oscillation between a loopback configuration and a no-transmission configuration of said cross-connection means, using a configuration controller.

21. (New) A method according to claim 20, further comprising providing a central clock signal using a central clock generator, wherein said start of cell signal generator, said offset controller, and said configuration controller each comprise an input port for said central clock signal.